CLAIMS

What is claimed is:

1. A method of integrated circuit design, said method comprising the steps of:

a) identifying critical paths in an integrated circuit design;

b) weighting edges in identified said critical paths

c) assigning net criticality to each weighted edge responsive to edge weight; and

d) re-placing and wiring nets according to edge criticality.

2. A method as in claim 1, further comprising before the step (a) of identifying critical paths, the step of:

a1) placing and wiring said integrated circuit design.

3. A method as in claim 2 wherein the step (a) of identifying critical paths further comprises removing non-critical paths from consideration.

4. A method as in claim 3 wherein step (b) of identifying critical paths comprises forming a slack graph indicating path slack and edges within said critical paths, non-critical paths being deleted from said slack graph.

5. A method as in claim 4 wherein step (c) of weighting edges comprises the steps of:

i) traversing said critical paths from front to back, an input path weight being assigned to each edge encountered in said traversal;

ii) traversing each critical path from back to front, an output path weight being assigned to each encountered edge in said reverse traversal; and

iii) summing said assigned input path weight and said assigned output path weight for each edge.

6. A method as in claim 5 wherein assigning net criticality value comprises:

sorting nets according to edge weight;

grouping sorted nets; and

assigning a criticality value to each group.

7. A method as in claim 6 wherein the step (c) of re-placing and wiring nets comprises:

i) selecting an edge having a highest criticality value;

ii) adjusting cell placement and net wiring for said selected edge; and

iii) checking for remaining critical edges and repeating steps i-ii until no critical edges are found.

8. A method as in claim 7 further including prior to the step (iii) of checking for remaining critical edges the step of:

iiiA) checking to determine if exit criteria are met and ending if said exit criteria are met.

9. A computer-readable medium having stored thereon a plurality of instructions, the plurality of instructions including instructions which, when executed by a processor, cause the processor to:

a) identify critical paths in an integrated circuit design;

b) weight edges in identified said critical path;

c) assign net criticality to each weighted edge responsive to edge weight; and

d) re-place and wire nets according to edge criticality.

10. A computer readable medium as in claim 9, identifying critical paths of step (a) causing the processor to:

a1) place and wire said integrated circuit design.

11. A computer readable medium as in claim 10 wherein the step (a) of identifying critical paths removes non-critical paths from consideration.

12. A computer readable medium as in claim 11 wherein identifying critical paths comprises forming a slack graph indicating path slack and edges within said critical paths, non-critical paths being deleted from said slack graph.

13. A computer medium as in claim 12 wherein step (c) of weighting edges causes the processor to:

i) traverse said critical paths from front to back and assign an input path weight to each edge encountered in said traversal;

ii) traverse each critical path from back to front and assign an output path weight to each encountered edge in said reverse traversal; and

iii) sum said assigned input path weight and said assigned output path weight for each edge.

14. A computer readable medium as in claim 13 wherein assigning criticality causes the processor to:

sort nets according to edge weight;

group sorted nets; and

assign a criticality value to each group.

15. A computer readable medium as in claim 14 wherein re-placing and wiring nets causes the processor to:

i) select an edge having a highest criticality value;

ii) adjust cell placement and net wiring for said selected edge; and

iii) check for remaining critical edges and repeat i-ii until no critical edges are found.

16. A computer medium as in claim 15 wherein if exit criteria are met, said processor is caused to end prior to selecting and adjusting all critical edges.